

# ESD132-B1-W0201

Bi-directional ESD protection device, 3.3 V, 0.45 pF, 0201

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## Product description

This Infineon ESD (electrostatic discharge) protection device has a bi-directional and symmetric  $I/V$  characteristic and excellent clamping performance.

## Feature list

- ESD / transient protection according to:
  - IEC61000-4-2 (ESD):  $\pm 30$  kV (air) /  $\pm 30$  kV (contact)
  - IEC61000-4-4 (EFT):  $\pm 4$  kV /  $\pm 80$  A (5/50 ns)
  - IEC61000-4-5 (Surge):  $\pm 9$  A (8/20  $\mu$ s)
- Bi-directional maximum working voltage:  $V_{WM} = \pm 5.5$  V
- Line capacitance:  $C_L = 0.45$  pF at  $f = 1$  MHz
- Clamping voltage:  $V_{cl} = 7$  V at  $I_{TLP} = 16$  A with  $R_{dyn} = 0.19 \Omega$
- Very low leakage current:  $I_L < 100$  nA
- Small form factor SMD size 0201, low profile (0.58 x 0.28 x 0.15 mm<sup>3</sup>)



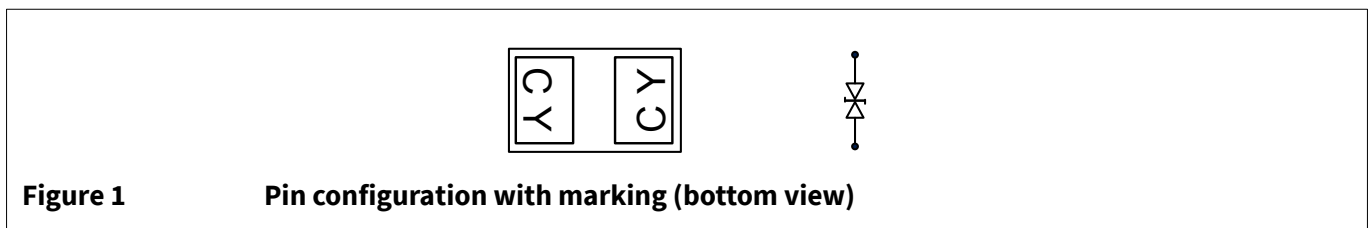
## Potential applications

- USB 3.x Gen 1
- HDMI, DisplayPort
- Ethernet

## Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

## Device information



**Table 1** Part information

Product name / Ordering code	Package	Pin configuration	Marking	Pieces / Reel
ESD132-B1-W0201 / ESD132B1W0201E6327XTSA1	WLL_2-3	1 line, bi-directional	CY	15 k

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## 1 Absolute maximum ratings

### 1 Absolute maximum ratings

**Table 2** Absolute maximum ratings at  $T_A = 25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Values		Unit	Note or test condition
		Min.	Max.		
Working voltage	$V_{WM}$	-5.5	+5.5	V	
ESD discharge voltage	$V_{ESD}$ (contact)	-30	+30	kV	Discharge network: $R = 330 \Omega$ , $C = 150 \text{ pF}$ <sup>1)</sup>
	$V_{ESD}$ (air)	-30	+30		
Peak pulse power	$P_{PK}$	-	63	W	Stress pulse: 8/20 $\mu\text{s}$ current waveform <sup>2)</sup>
Peak pulse current	$I_{PP}$	-9	+9	A	
Operating temperature	$T_{op}$	-55	+125	$^\circ\text{C}$	
Storage temperature	$T_{stg}$	-65	+150		

**Attention:** Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings. Exceeding only one of these values may cause irreversible damage to the component.

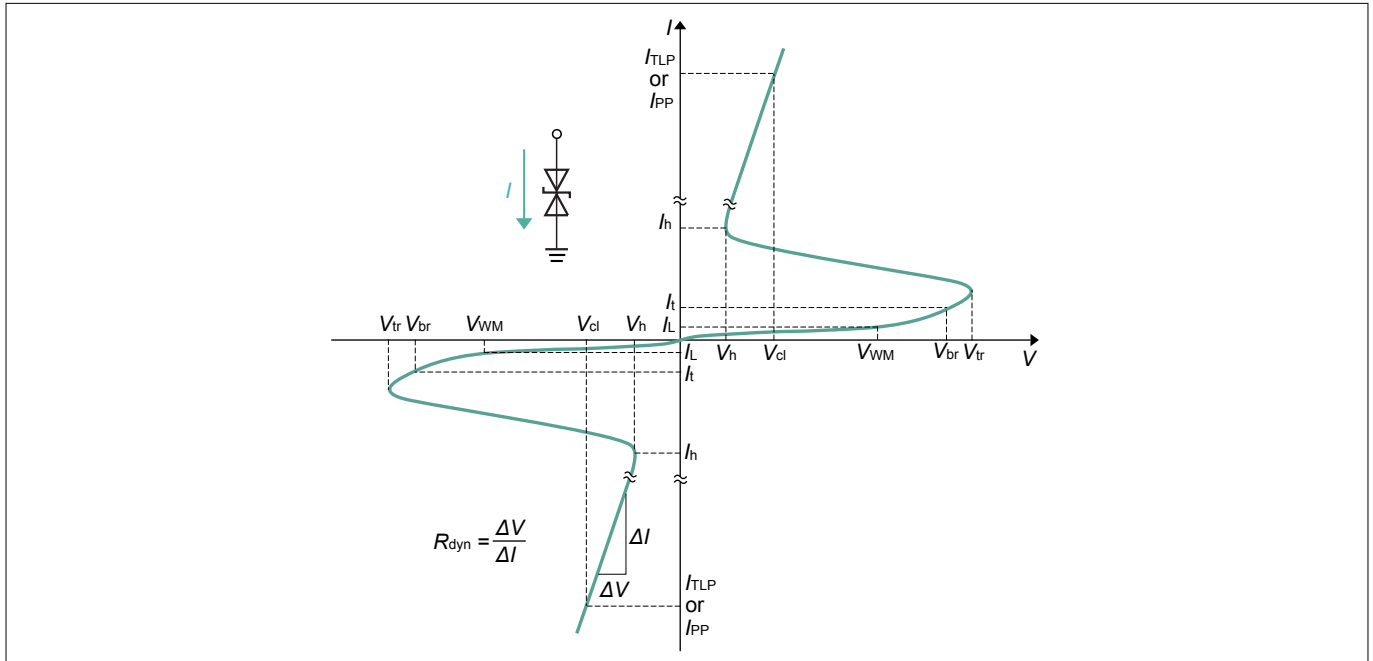
<sup>1</sup> Based on IEC61000-4-2.

<sup>2</sup> Based on IEC61000-4-5.

**2 Electrical characteristics**

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Note:  $T_A = 25^\circ\text{C}$ , unless otherwise specified. Device is electrically symmetrical.



**Figure 2** I/V characteristic curve

**Table 3** I/V characteristic parameters

Symbol	Parameter
$I_h$	Holding current
$I_L$	Leakage current
$I_{PP}$	Peak pulse current, based on IEC61000-4-5
$I_t$	Test current
$I_{TLP}$	TLP current
$R_{dyn}$	Dynamic resistance
$V_{br}$	Breakdown voltage
$V_{cl}$	Clamping voltage
$V_h$	Holding voltage
$V_t$	Test voltage
$V_{tr}$	Trigger voltage
$V_{WM}$	Maximum working voltage

Note: For more detailed explanation of electrical parameters refer to [\[1\]](#)

## 2 Electrical characteristics

**Table 4 DC characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Breakdown voltage	$V_{br}$	6.1	8.5	–	V	$I_t = 1 \text{ mA}$
Holding voltage	$V_h$	–	1.8	–		$I = I_h$
Holding current	$I_h$	–	30	–	mA	$V = V_h$
Leakage current	$I_L$	–	–	100	nA	$V_{WM} = 5.5 \text{ V}$

**Table 5 AC characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Line capacitance	$C_L$	–	0.45	0.55	pF	$V = 0 \text{ V}, f = 1 \text{ MHz}$
Series inductance	$L_S$	–	<0.1	–	nH	

**Table 6 Protection characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Clamping voltage (TLP) <sup>3) 4)</sup>	$V_{cl}$	–	5.5	–	V	$I_{TLP} = 8 \text{ A}$
		–	7	–		$I_{TLP} = 16 \text{ A}$
		–	9.5	–		$I_{TLP} = 30 \text{ A}$
Clamping voltage (8/20 $\mu\text{s}$ ) <sup>5) 6)</sup>		–	3	–		$I_{PP} = 1 \text{ A}$
		–	6	8		$I_{PP} = 8 \text{ A}$
Dynamic resistance <sup>3)</sup>	$R_{dyn}$	–	0.19	–	$\Omega$	

<sup>3)</sup> TLP parameters:  $Z_0 = 50 \Omega$ ,  $t_p = 100 \text{ ns}$ ,  $t_r = 0.6 \text{ ns}$ , averaging window 30-60 ns.

<sup>4)</sup> Refer to application note AN210 [2]

<sup>5)</sup>  $t_p = 8/20 \mu\text{s}$ . Stress pulse based on IEC61000-4-5.

<sup>6)</sup> Verified by design.

3 Typical characteristic diagrams

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Note:  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified.

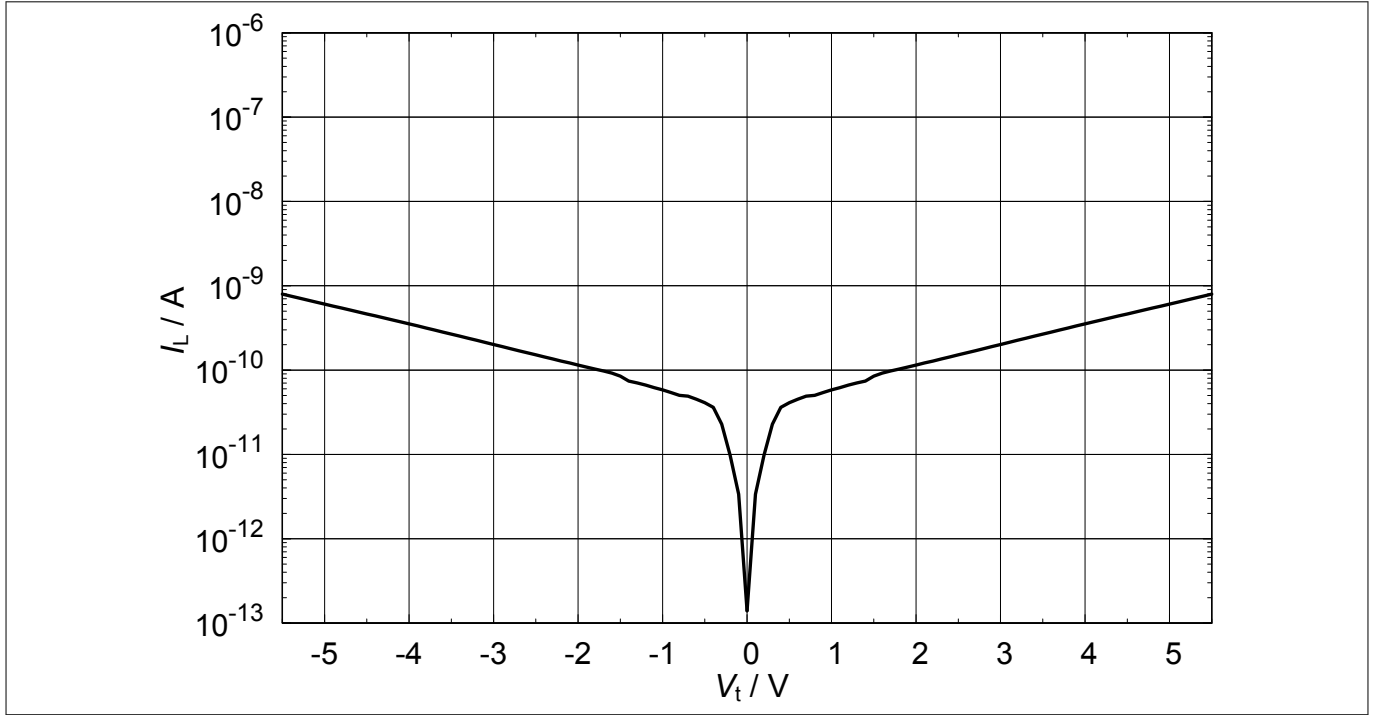


Figure 3 Leakage current:  $I_L = f(V_t)$

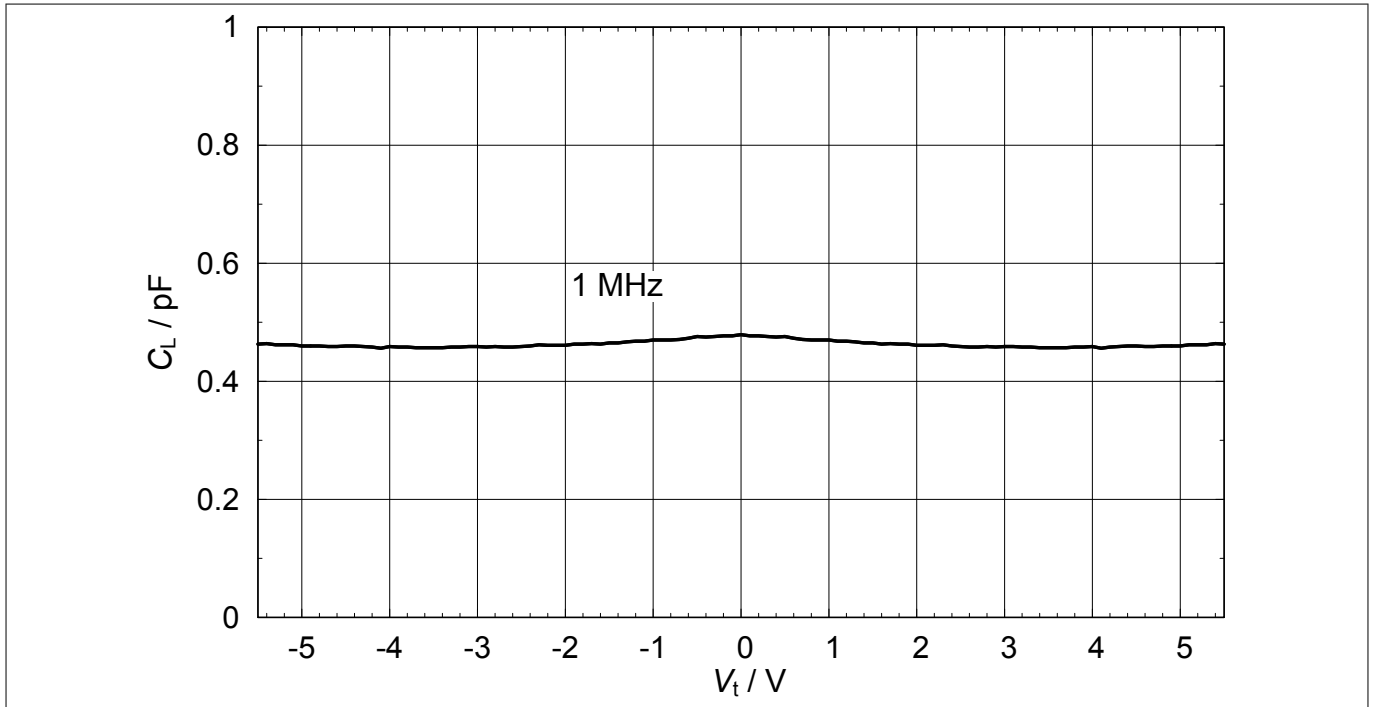
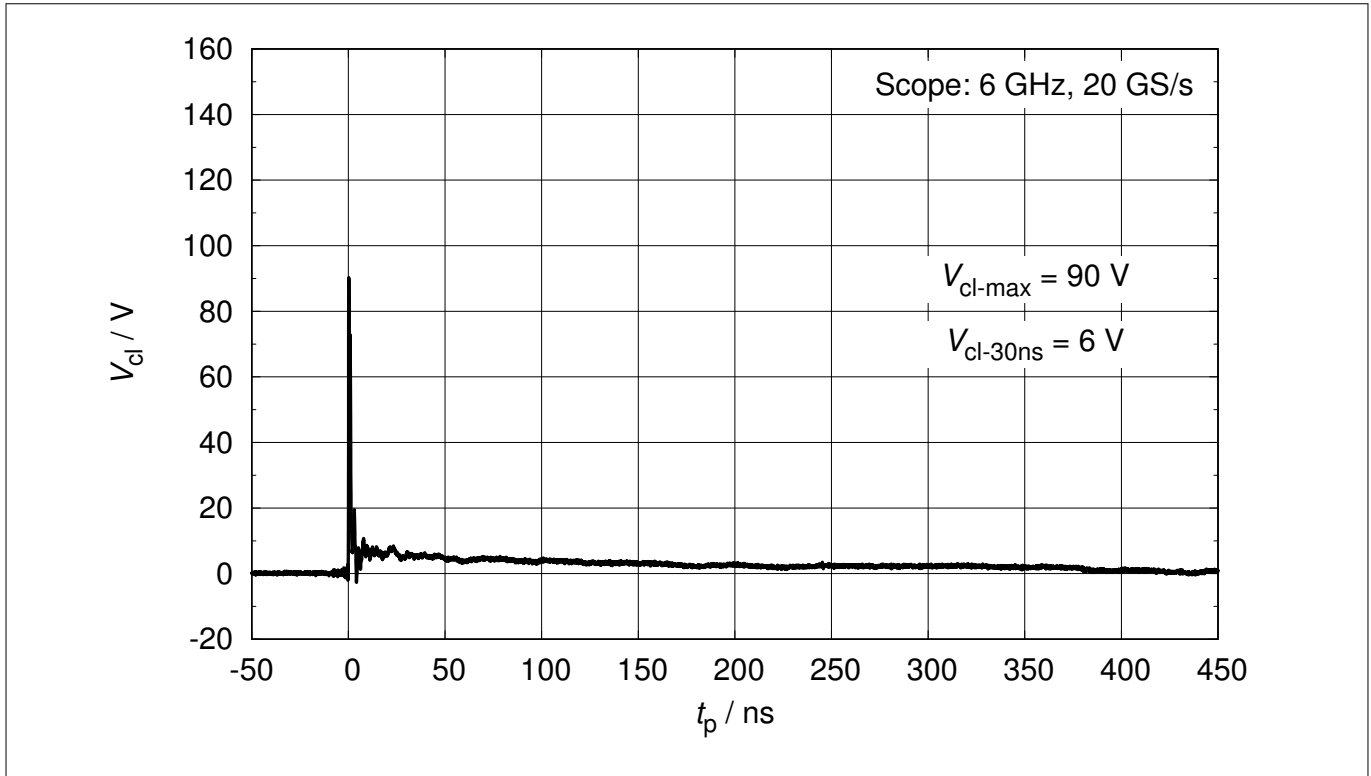
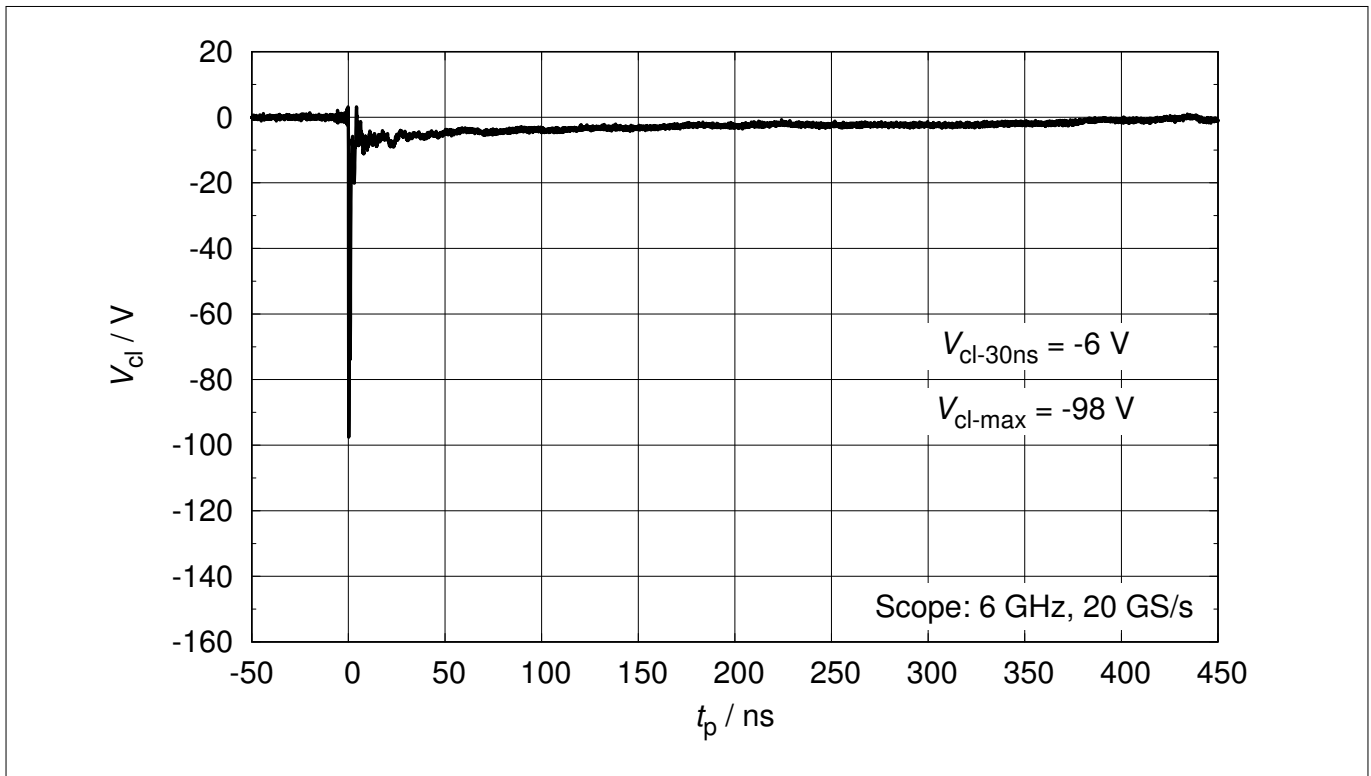


Figure 4 Line capacitance:  $C_L = f(V_t)$ ,  $f = 1\text{ MHz}$

**3 Typical characteristic diagrams**

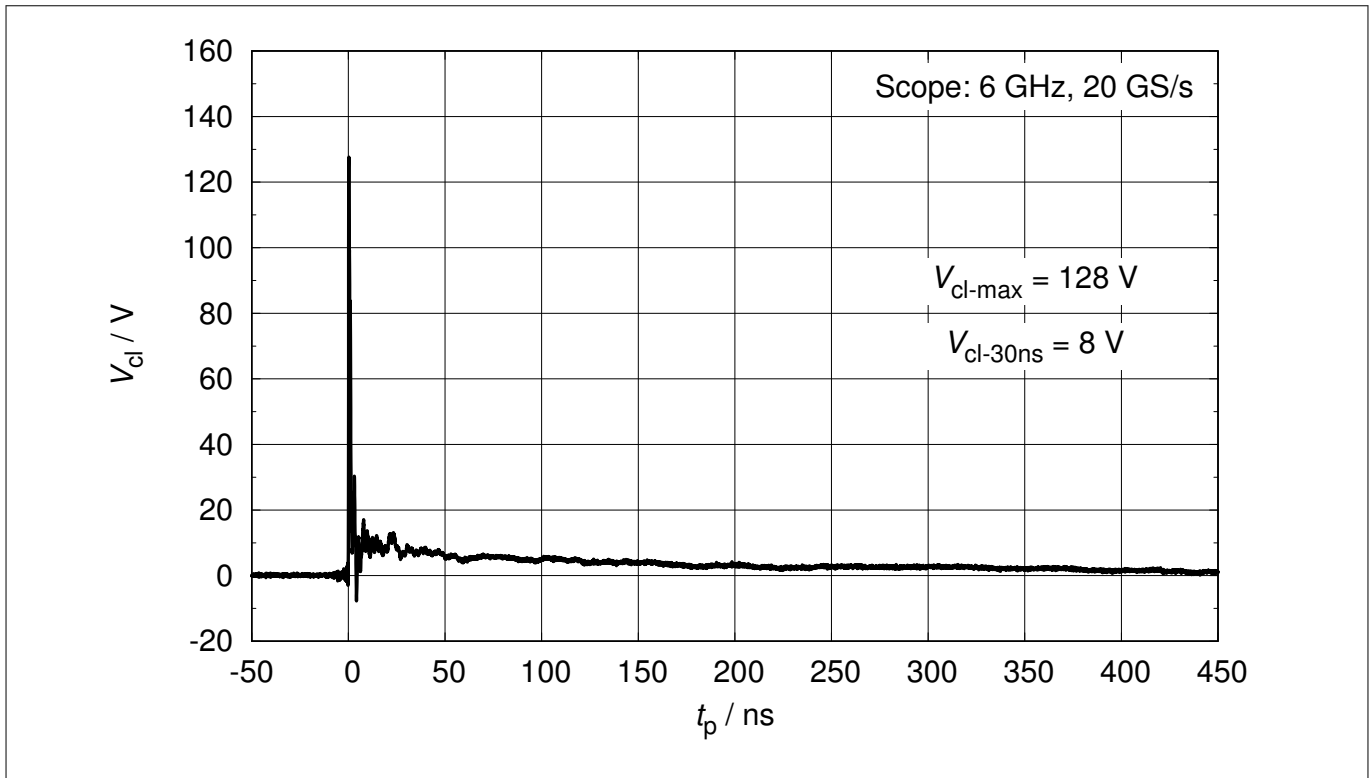


**Figure 5 Clamping voltage (ESD):  $V_{cl} = f(t_p)$ , 8 kV positive pulse based on IEC61000-4-2**

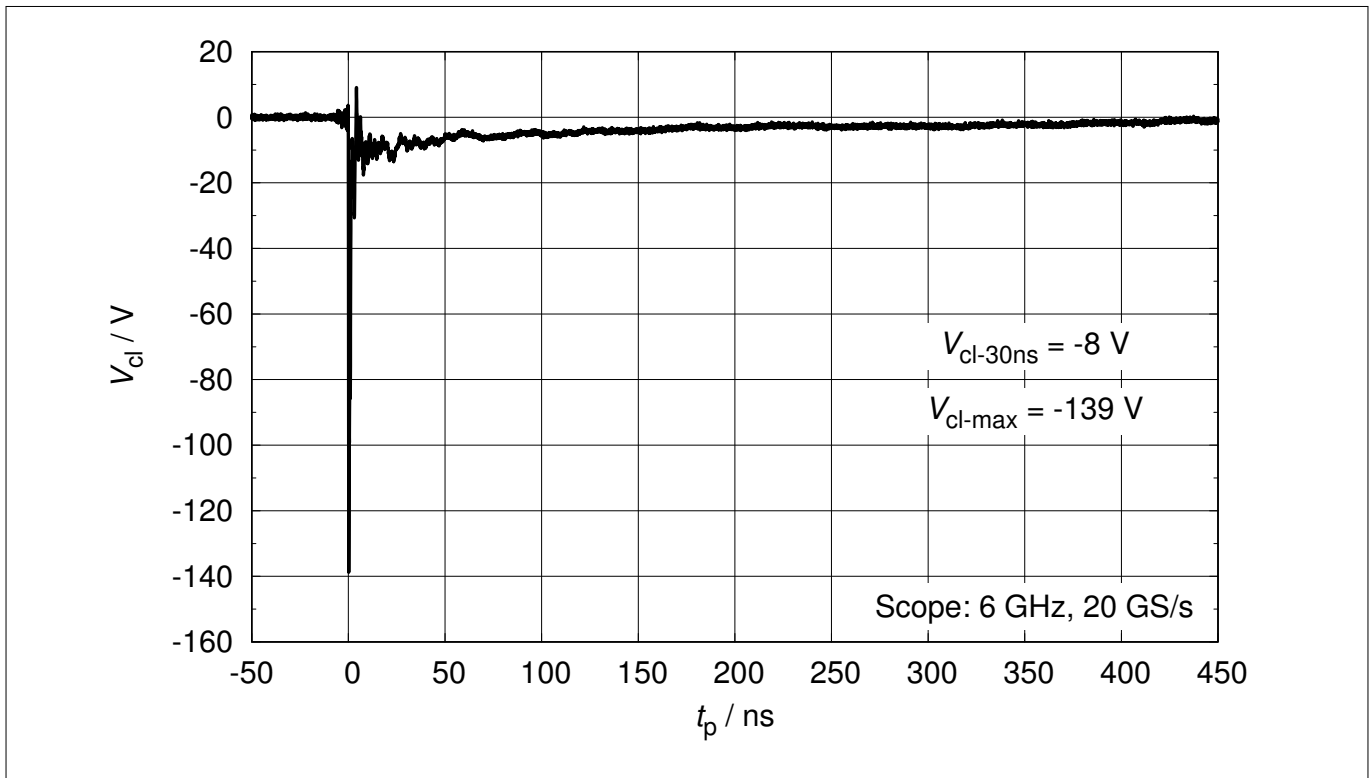


**Figure 6 Clamping voltage (ESD):  $V_{cl} = f(t_p)$ , 8 kV negative pulse based on IEC61000-4-2**

**3 Typical characteristic diagrams**

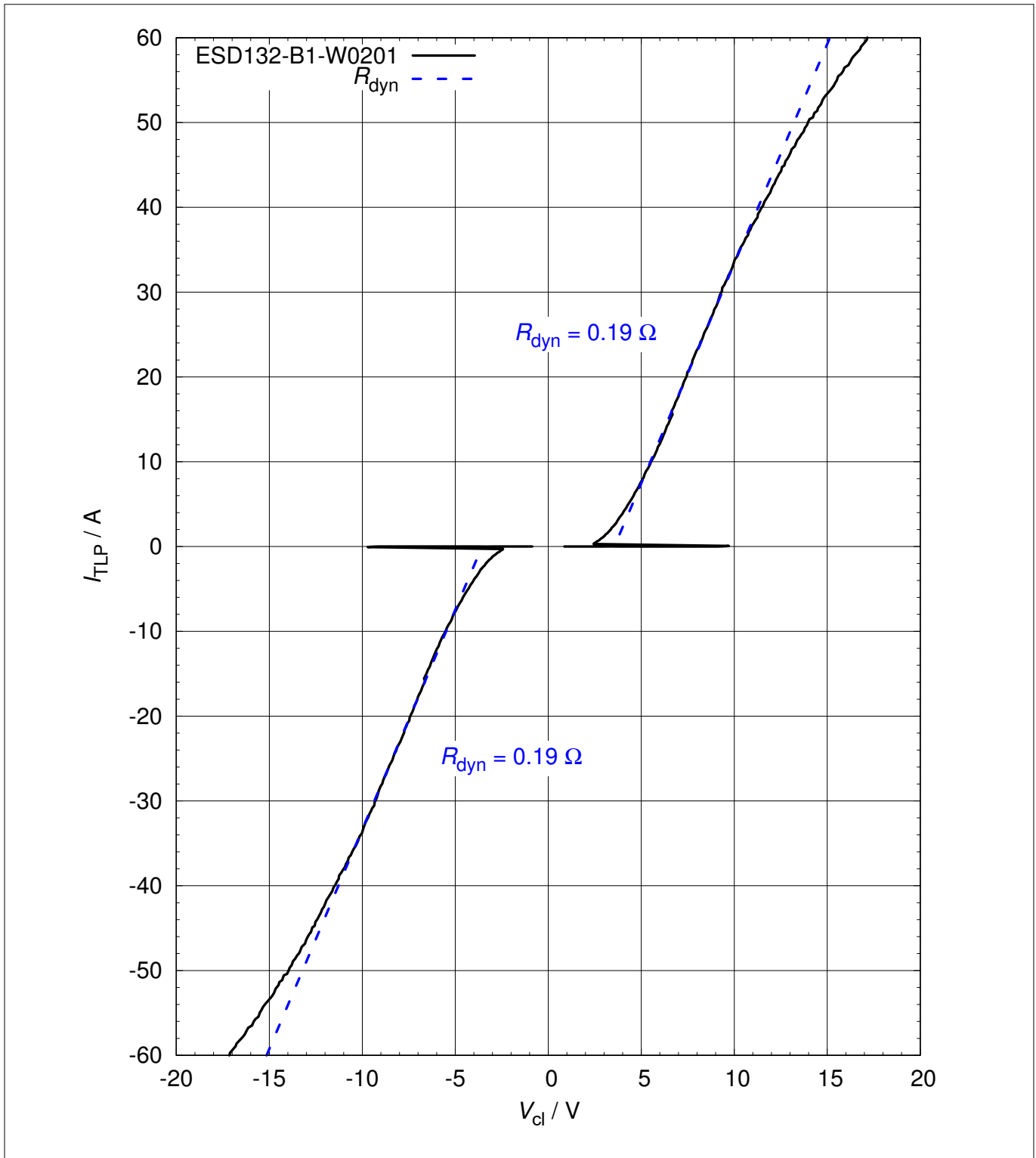


**Figure 7 Clamping voltage (ESD):  $V_{cl} = f(t_p)$ , 15 kV positive pulse based on IEC61000-4-2**



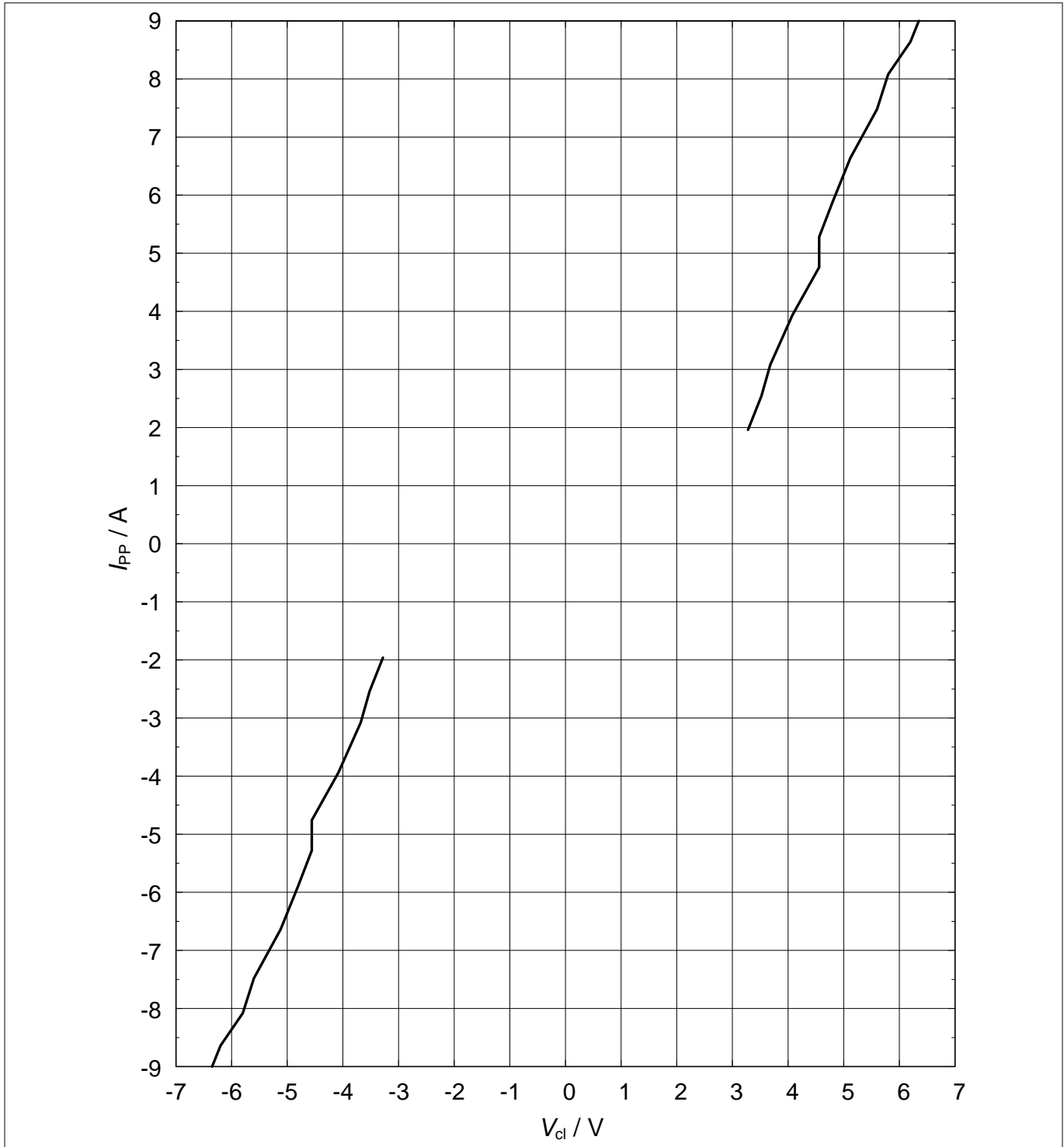
**Figure 8 Clamping voltage (ESD):  $V_{cl} = f(t_p)$ , 15 kV negative pulse based on IEC61000-4-2**

**3 Typical characteristic diagrams**



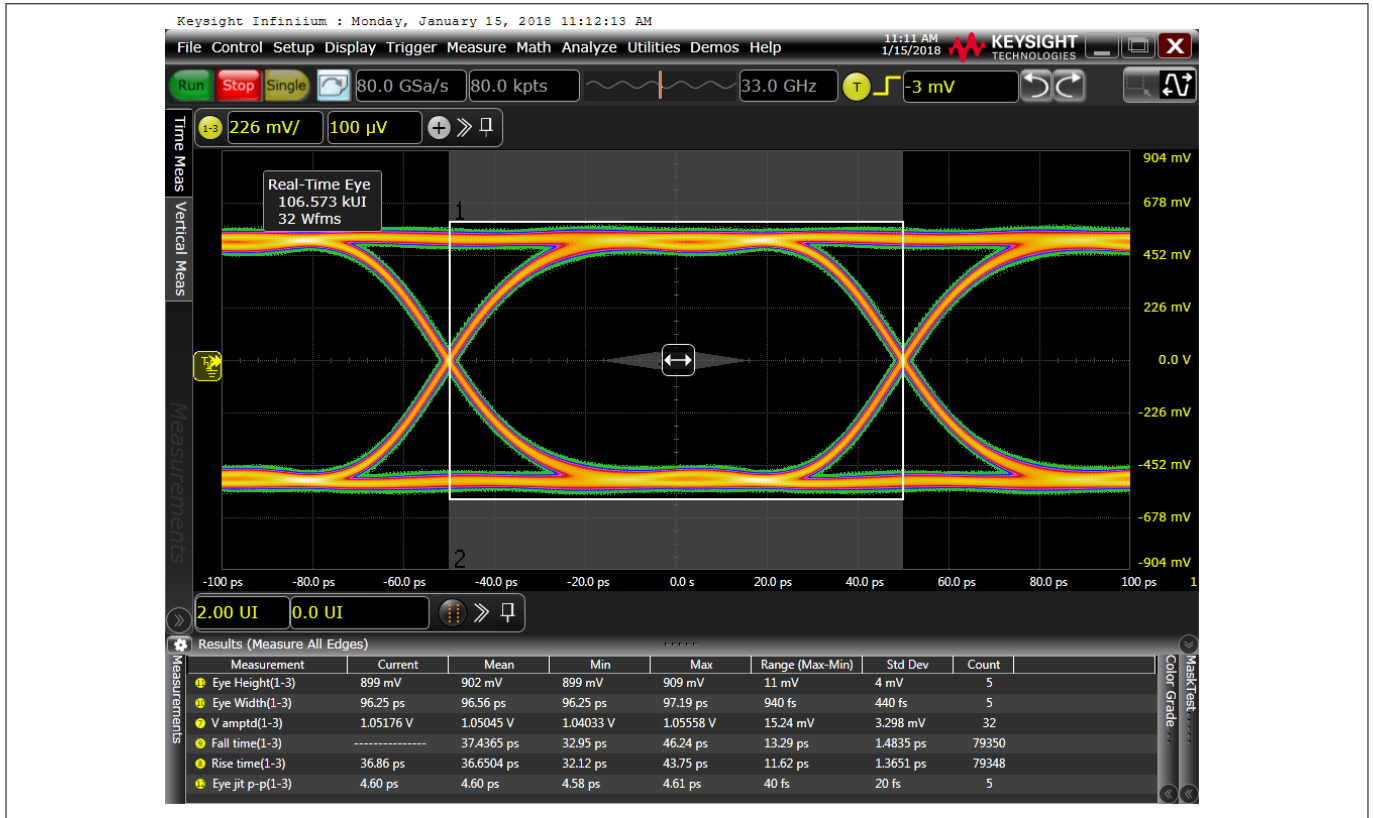
**Figure 9** Clamping voltage (TLP):  $I_{TLP} = f(V_{cl})$

**3 Typical characteristic diagrams**

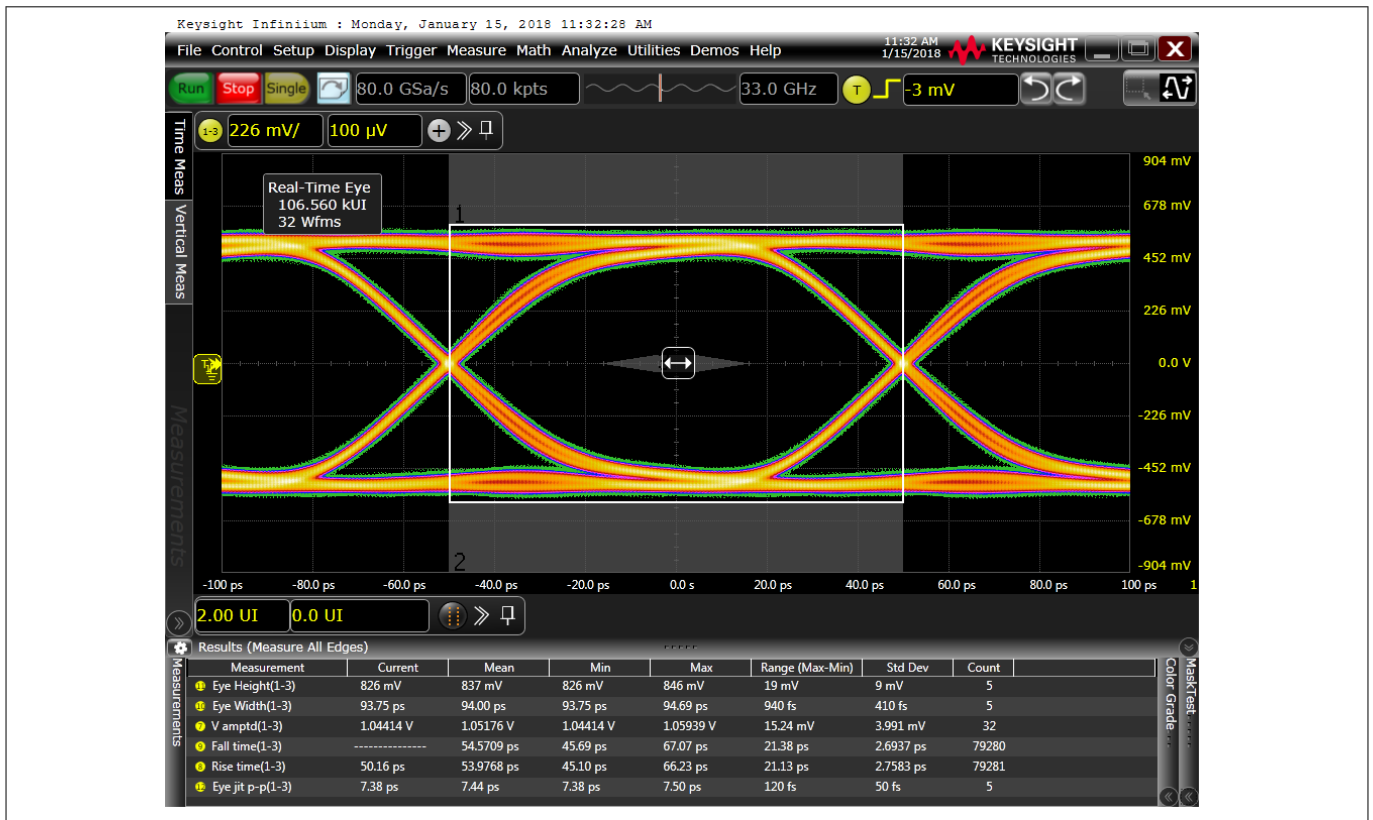


**Figure 10** Clamping voltage (Surge):  $I_{PP} = f(V_{cl})$ , based on IEC61000-4-5

**3 Typical characteristic diagrams**

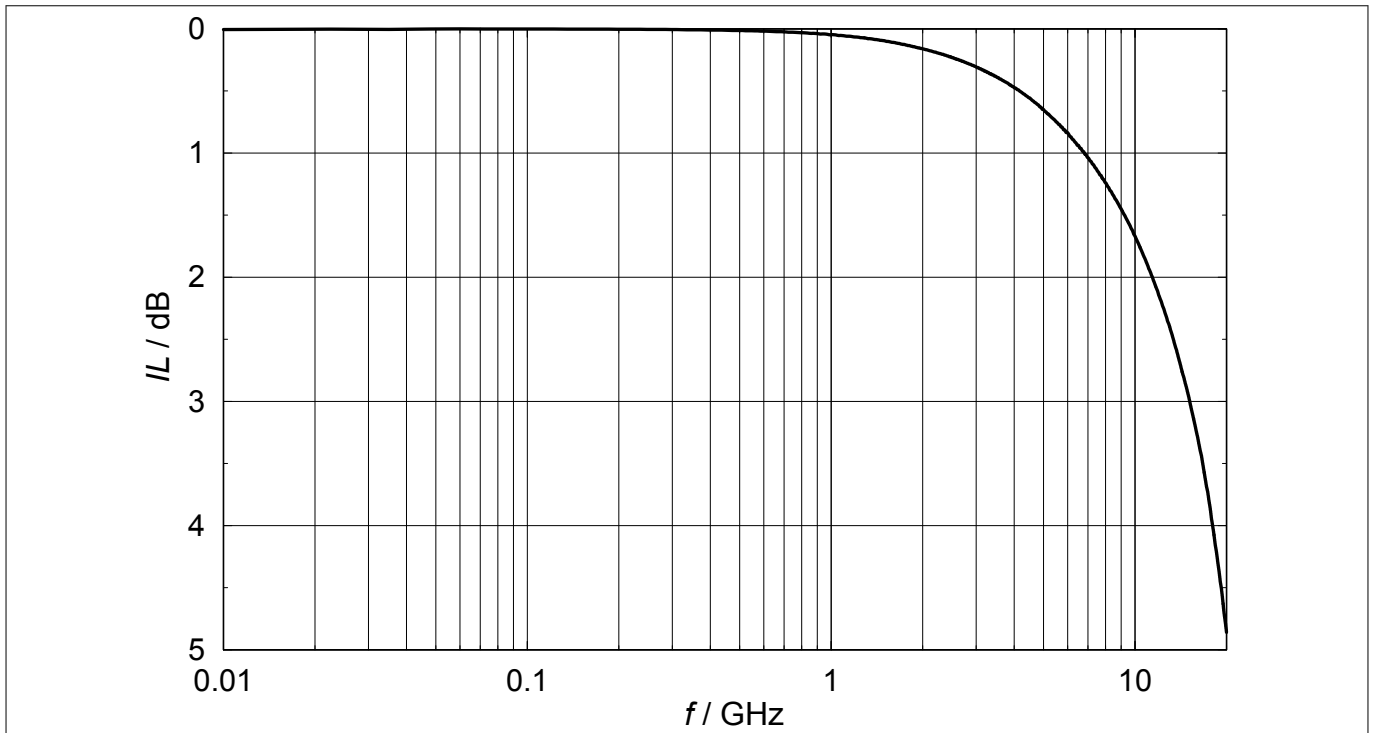


**Figure 11 10 Gbps Eye diagram with USB 3.1/3.2 Gen 2 Mask, test board only**



**Figure 12 10 Gbps Eye diagram with USB 3.1/3.2 Gen 2 Mask, test board + ESD132-B1-W0201**

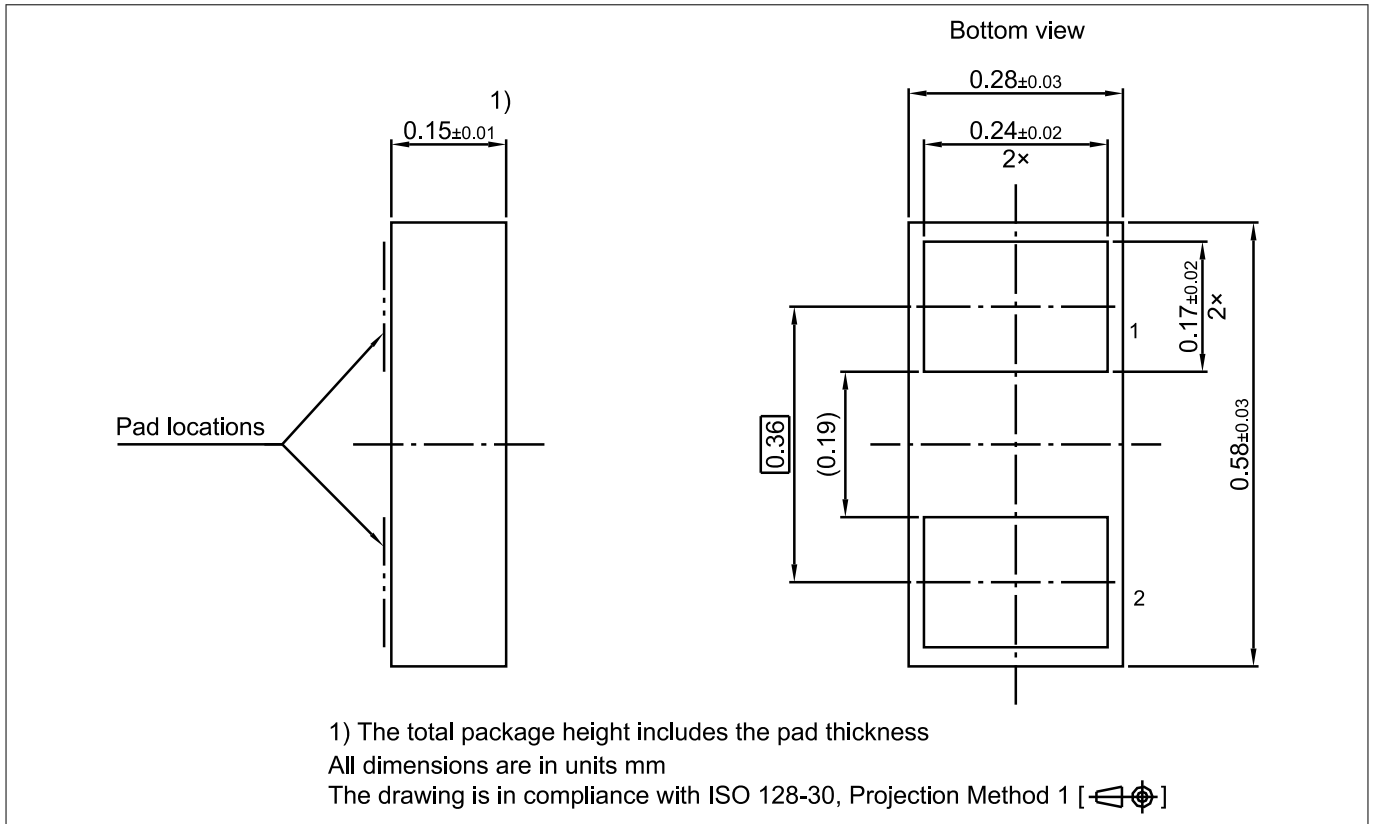
**3 Typical characteristic diagrams**



**Figure 13** Insertion loss  $IL = f(f)$ , measured in a 50  $\Omega$  system

**4 Package information WLL-2-3**

**4 Package information WLL-2-3**



**Figure 14 WLL-2-3 package**

Note: For package information including footprint, packing and assembly recommendation refer to:

<https://www.infineon.com/packages/SG-WLL-2-3/>

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**5 References**
**5 References**

[1]	Infineon AG - Understanding ESD protection device characteristics
[2]	Infineon AG - <b>Application note AN210</b> : Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology

**6 Revision history**

Document version	Date of release	Description of changes
0.9	2018-02-06	<ul style="list-style-type: none"> <li>First release</li> </ul>
1.0	2018-06-26	<ul style="list-style-type: none"> <li>Typical and maximum values updated to production values</li> <li>Typical curves updated to production values</li> <li><math>V_{CL}</math> pulse curves and eye diagrams added</li> <li>Minor editorial changes</li> </ul>
2.0	2019-08-09	<ul style="list-style-type: none"> <li>New datasheet layout</li> </ul>
3.0	2020-11-30	<ul style="list-style-type: none"> <li>Editorial changes</li> </ul>

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